

## USER MANUAL

# Accessory 68E

UMAC I/O Board

3Ax-603595-xUxx

January 27, 2003



Single Source Machine Control

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## **SCHEMATIC**

## INTRODUCTION

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The UMAC Accessory 68E is a general-purpose input/output board to the UMAC-Turbo or UMAC MACRO systems. Both the inputs and outputs of this board are to be configured as **Sinking signals ONLY**. ACC-68E provides 24 lines of self protected ***optically isolated*** inputs and 24 lines of self protected ***optically isolated*** outputs. The actual I/O Reads are carried out using M-variables, which will be described later. ACC-68E is one of the series of 3U rack I/O accessories designed to transfer data through the UMAC BUS (UBUS). Other boards in the family of the UMAC I/O Accessory products include the following:

<b>ACC-9E</b>	48 optically isolated inputs
<b>ACC-10E</b>	48 optically isolated outputs, low power
<b>ACC-11E</b>	24 inputs and 24 outputs, low power, all optically isolated
<b>ACC-12E</b>	24 inputs and 24 outputs, high power, all optically isolated
<b>ACC-14E</b>	48-bits TTL level I/O
<b>ACC-65E</b>	Sourcing 24 inputs and 24 outputs, self protecting, all optically isolated, 250mA outputs
<b>ACC-66E</b>	48 optically isolated, self protecting, sourcing inputs
<b>ACC-67E</b>	48 optically isolated, self protecting, sourcing outputs, 250mA outputs
<b>ACC-68E</b>	Sinking 24 inputs and 24 outputs, self protecting, all optically isolated

The inputs to the ACC-68E board have an activation range from 12V to 24V. Due to the self-protecting circuitry, the inputs can only be configured as sinking inputs. Although self-protecting there are still limits to power supplied to the inputs of the ACC-68E. The limiting voltages are  $V_f = 57$  volts input to the I/O and the  $V_r = 33$  volts input to the I/O. These limitations are due to the protective circuitry including the MMBZ33VALT1 Zener diodes.

The output drivers are organized in a set of three 8-bit groups. The output chip used for the sinking configuration is the ULN2803. Each open collector output line can sink up to 100mA when pulled up to a voltage level between 12 and 24 volts (external pull-up resistors are not supplied).

## HARDWARE SETUP

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The ACC-68E uses expansion port memory locations defined by the type of PMAC (3U Turbo or MACRO Station) it is directly communicating to. These memory locations are typically used with other Delta Tau 3U I/O accessories such as:

ACC-9E, ACC-10E, ACC-11E	ACC-12E
ACC-65E, ACC66E, ACC-67E, ACC-68E	
ACC-28E	16-bit A/D Converter Inputs (up to four per card)
ACC-53E	SSI Encoder Inputs

All of these accessories have settings, which tell them where the information is to be processed at either the PMAC 3U Turbo or the MACRO Station.

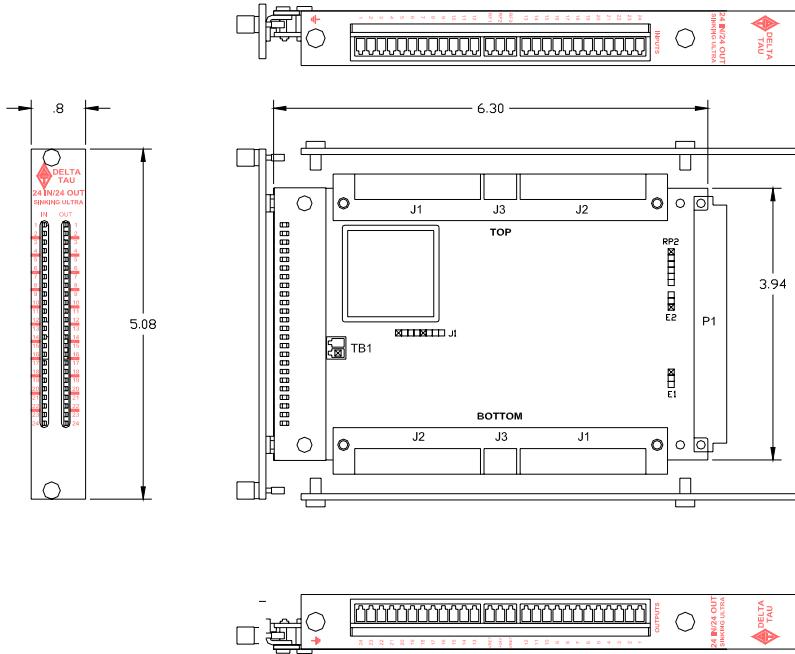
3U Turbo PMAC Memory Locations	MACRO Station Memory Locations
\$078C00, \$079C00	\$8800,\$9800
\$07AC00, \$07BC00	\$A800,\$B800
\$078D00, \$079D00	\$8840,\$9840
\$07AD00, \$07BD00	\$A840,\$B840
\$078E00, \$079E00	\$8880,\$9880
\$07AE00, \$07EC00	\$A880,\$B880
\$078F00, \$079F00	\$88C0,\$98C0
\$07AF00, \$07BF00	\$A8C0,\$B8C0

The ACC-68E has a set of dip-switches telling it where to process its data. Once the information is at these locations, we can process the binary word in the encoder conversion table to use for servo loop closure. Proper setting of the dip-switches ensures all of the UBUS IO boards used in the application do not interfere with each other.

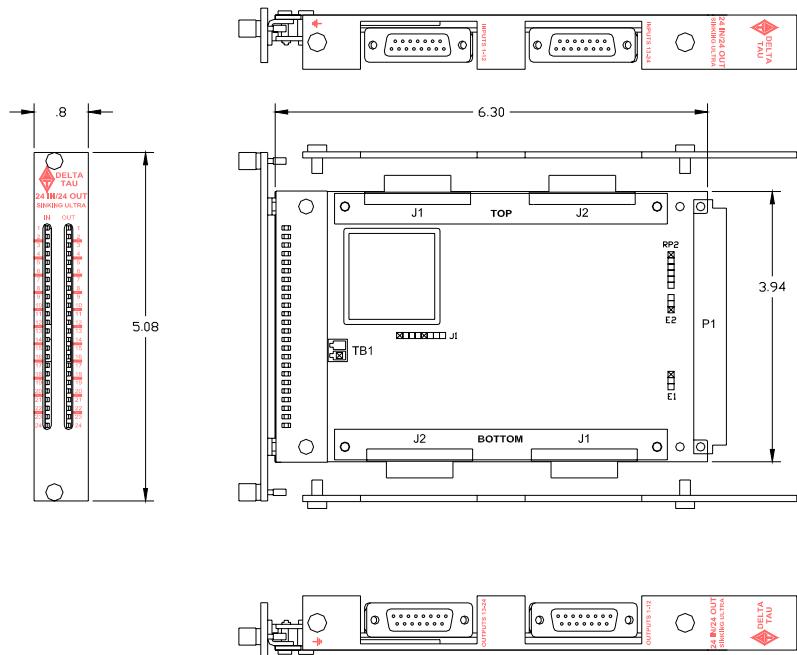
## Layout Diagram

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### ACC-68E Terminal Block Option



### ACC-68E DB15 Option



## Address Select DIP Switch S1

The switch one (S1) settings will allow the user to select the starting address location for the first IO gate on the ACC-68E. The following two tables show the dip switch settings for both the TURBO PMAC 3U and the MACRO Station.

### TURBO PMAC 3U Switch Settings

CHIP SELECT	3U Turbo PMAC Address	DIP SWITCH SW1 POSITION					
		6	5	4	3	2	1
CS10	Y:\$78C00-03	CLOSE	CLOSE	CLOSE	CLOSE	CLOSE	CLOSE
	Y:\$79C00-03	CLOSE	CLOSE	CLOSE	OPEN	CLOSE	CLOSE
	Y:\$7AC00-03	CLOSE	CLOSE	OPEN	CLOSE	CLOSE	CLOSE
	Y:\$7BC00-03	CLOSE	CLOSE	OPEN	OPEN	CLOSE	CLOSE
CS12	Y:\$78D00-03	CLOSE	CLOSE	CLOSE	CLOSE	CLOSE	OPEN
	Y:\$79D00-03	CLOSE	CLOSE	CLOSE	OPEN	CLOSE	OPEN
	Y:\$7AD00-03	CLOSE	CLOSE	OPEN	CLOSE	CLOSE	OPEN
	Y:\$7BD00-03	CLOSE	CLOSE	OPEN	OPEN	CLOSE	OPEN
CS14	Y:\$78E00-03	CLOSE	CLOSE	CLOSE	CLOSE	OPEN	CLOSE
	Y:\$79E00-03	CLOSE	CLOSE	CLOSE	OPEN	OPEN	CLOSE
	Y:\$7AE00-03	CLOSE	CLOSE	OPEN	CLOSE	OPEN	CLOSE
	Y:\$7BE00-03	CLOSE	CLOSE	OPEN	OPEN	OPEN	CLOSE
CS16	Y:\$78F00-03	CLOSE	CLOSE	CLOSE	CLOSE	OPEN	OPEN
	Y:\$79F00-03	CLOSE	CLOSE	CLOSE	OPEN	OPEN	OPEN
	Y:\$7AF00-03	CLOSE	CLOSE	OPEN	CLOSE	OPEN	OPEN
	Y:\$7BF00-03	CLOSE	CLOSE	OPEN	OPEN	OPEN	OPEN

### MACRO Station Switch Settings

CHIP SELECT	3U Turbo PMAC Address	DIP SWITCH SW1 POSITION					
		6	5	4	3	2	1
CS10	Y:\$8800	CLOSE	CLOSE	CLOSE	CLOSE	CLOSE	CLOSE
	Y:\$9800	CLOSE	CLOSE	CLOSE	OPEN	CLOSE	CLOSE
	Y:\$A800	CLOSE	CLOSE	OPEN	CLOSE	CLOSE	CLOSE
	Y:\$B800 (\$FFE0*)	CLOSE	CLOSE	OPEN	OPEN	CLOSE	CLOSE
CS12	Y:\$8840	CLOSE	CLOSE	CLOSE	CLOSE	CLOSE	OPEN
	Y:\$9840	CLOSE	CLOSE	CLOSE	OPEN	CLOSE	OPEN
	Y:\$A840	CLOSE	CLOSE	OPEN	CLOSE	CLOSE	OPEN
	Y:\$B840 (\$FFE8*)	CLOSE	CLOSE	OPEN	OPEN	CLOSE	OPEN
CS14	Y:\$8880	CLOSE	CLOSE	CLOSE	CLOSE	OPEN	CLOSE
	Y:\$9880	CLOSE	CLOSE	CLOSE	OPEN	OPEN	CLOSE
	Y:\$A880	CLOSE	CLOSE	OPEN	CLOSE	OPEN	CLOSE
	Y:\$B880 (\$FFF0*)	CLOSE	CLOSE	OPEN	OPEN	OPEN	CLOSE
CS16	Y:\$88C0	CLOSE	CLOSE	CLOSE	CLOSE	OPEN	OPEN
	Y:\$98C0	CLOSE	CLOSE	CLOSE	OPEN	OPEN	OPEN
	Y:\$A8C0	CLOSE	CLOSE	OPEN	CLOSE	OPEN	OPEN
	Y:\$B8C0	CLOSE	CLOSE	OPEN	OPEN	OPEN	OPEN

The default setting is **ALL CLOSED** position.

## Jumpers

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Please refer to the layout diagram of ACC-68E for the location of the jumpers on the board.

### E-Point Jumpers

Jumper	Config	Description	Settings	Default
E1	1-2	Turbo-PMAC/MACRO Select	Jump 1-2 for Turbo 3U CPU and MACRO CPU * Jump 2-3 for legacy MACRO CPU (before 6/00)	1-2
E2	1-2	Sample Clock Select	1-2 servo clock 2-3 phase clock	1-2

\* for legacy MACRO Stations (part number 602804-100 thru 602804-104)

## Hardware Address Limitations

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Some of the older UMAC IO accessories might create a hardware address limitation relative to the newer series of UMAC high speed IO cards. The ACC-66E would be considered a newer high speed IO card. The new IO cards have four addresses per chip select (CS10, CS12, CS14, and CS16). This enables these cards to have up to 16 different addresses. The ACC-9E, ACC-10E, ACC-11E, and ACC-12E all have one address per chip select but also have the low-byte, middle-byte, and high-byte type of addressing scheme and allows for a maximum of twelve of these IO cards.

### UMAC Card Types

UMAC CARD	Number of Addresses	Category	Maximum # of cards	Card Type
ACC-9E , ACC-10E ACC-11E, ACC-12E	4	General IO	12	<b>A</b>
ACC-65E, ACC-66E ACC-67E, ACC-68E ACC-14E	16	General IO	16	<b>B</b>
ACC-28E, ACC-36E ACC-59E	16	ADC and DAC	16	<b>B</b>
ACC-53E, ACC-57E ACC-58E	16	Feedback Devices	16	<b>B</b>

### Chip Select Addresses

Chip Select	UMAC Turbo Type A Card	MACRO Type A Card	UMAC Turbo Type B Card	MACRO Type B Card
10	\$078C00	\$FFE0 or \$8800	\$078C00, \$079C00 \$07AC00, \$07BC00	\$8800,\$9800 \$A800,\$B800
12	\$078D00	\$FFE8 or \$8840	\$078D00, \$079D00 \$07AD00, \$07BD00	\$8840,\$9840 \$A840,\$B840
14	\$078E00	\$FFF0 or \$8880	\$078E00, \$079E00 \$07AE00, \$07EC00	\$8880,\$9880 \$A880,\$B880
16	\$078F00	\$88C0	\$078F00, \$079F00 \$07AF00, \$07BF00	\$88C0,\$98C0 \$A8C0,\$B8C0

## **Addressing Conflicts**

When just using only the type A UMAC cards or using only the type B UMAC cards in an application, the user does not have to worry about potential addressing conflicts other than making sure the individual cards are set to the addresses as specified in the manual.

If the user has both type A and type B UMAC cards in their rack they should be aware of the possible addressing conflicts. If the customer is using the Type A card on a particular Chip Select (CS10, CS12, CS14, or CS16) then they cannot use a Type B card with the same Chip Select address unless the Type B card is a general IO type. If the Type B card is a general IO type, then the Type B card will be the low-byte card at the Chip Select address and the Type A card(s) will be setup at as the middle-byte and high-byte addresses.

### **Type A and Type B Example 1: ACC-11E and ACC-36E**

If the user has an ACC-11E and ACC-36E the user cannot allow both cards to use the same Chip Select because the data from both cards will be overwritten by the other card.

The solution to this problem is to make sure you do not address both cards to the same chip select.

### **Type A and Type B Example 2: ACC-11E and ACC-68E**

For this example the user could allow the two cards to share the same chip select because the ACC-68E is a general purpose IO Type B card. The only restriction in doing so is that the ACC-68E must be considered the low-byte addressed card and the ACC-11E must be jumpered to either the middle or high bytes (jumper E6A-E6H).



## USING ACC-68E WITH UMAC TURBO

For the UMAC-Turbo, the ACC-68E can be used for either general purpose I/O or as latched inputs. The registers used for general I/O use are 8-bit registers and you will define three 8-bit registers for each 24-bit I/O port.

### UMAC-Turbo Memory Mapping for ACC-68E

The Delta Tau I/O Gate used on the ACC-68E is an 8-bit processor and therefore the memory mapping to the I/O bits is processed as 8-bit words at the Turbo UMAC. Using this simple scheme the user could process up to 768 (48×16) bits of data for general purpose I/O.

	CS10 SW1-1 ON SW1-2 ON	CS12 SW1-1 OFF SW1-2 ON	CS14 SW1-1 ON SW1-2 OFF	CS16 SW1-1 OFF SW1-2 OFF	Description
SW1-3 ON SW1-4 ON	Y:\$078C00,0,8 Y:\$078C01,0,8 Y:\$078C02,0,8 Y:\$078C03,0,8 Y:\$078C04,0,8 Y:\$078C05,0,8 Y:\$078C07,0,8	Y:\$078D00,0,8 Y:\$078D01,0,8 Y:\$078D02,0,8 Y:\$078D03,0,8 Y:\$078D04,0,8 Y:\$078D05,0,8 Y:\$078D07,0,8	Y:\$078E00,0,8 Y:\$078E01,0,8 Y:\$078E02,0,8 Y:\$078E03,0,8 Y:\$078E04,0,8 Y:\$078E05,0,8 Y:\$078E07,0,8	Y:\$078F00,0,8 Y:\$078F01,0,8 Y:\$078F02,0,8 Y:\$078F03,0,8 Y:\$078F04,0,8 Y:\$078F05,0,8 Y:\$078F07,0,8	I/O bits 0-7 I/O bits 8-15 I/O bits 16-23 I/O bits 24-31 I/O bits 32-39 I/O bits 40-47 Control Word
SW1-3 OFF SW1-4 ON	Y:\$079C00,0,8 Y:\$079C01,0,8 Y:\$079C02,0,8 Y:\$079C03,0,8 Y:\$079C04,0,8 Y:\$079C05,0,8 Y:\$079C07,0,8	Y:\$079D00,0,8 Y:\$079D01,0,8 Y:\$079D02,0,8 Y:\$079D03,0,8 Y:\$079D04,0,8 Y:\$079D05,0,8 Y:\$079D07,0,8	Y:\$079E00,0,8 Y:\$079E01,0,8 Y:\$079E02,0,8 Y:\$079E03,0,8 Y:\$079E04,0,8 Y:\$079E05,0,8 Y:\$079E07,0,8	Y:\$079F00,0,8 Y:\$079F01,0,8 Y:\$079F02,0,8 Y:\$079F03,0,8 Y:\$079F04,0,8 Y:\$079F05,0,8 Y:\$079F07,0,8	I/O bits 0-7 I/O bits 8-15 I/O bits 16-23 I/O bits 24-31 I/O bits 32-39 I/O bits 40-47 Control Word
SW1-3 ON SW1-4 OFF	Y:\$07AC00,0,8 Y:\$07AC01,0,8 Y:\$07AC02,0,8 Y:\$07AC03,0,8 Y:\$07AC04,0,8 Y:\$07AC05,0,8 Y:\$07AC07,0,8	Y:\$07AD00,0,8 Y:\$07AD01,0,8 Y:\$07AD02,0,8 Y:\$07AD03,0,8 Y:\$07AD04,0,8 Y:\$07AD05,0,8 Y:\$07AD07,0,8	Y:\$07AE00,0,8 Y:\$07AE01,0,8 Y:\$07AE02,0,8 Y:\$07AE03,0,8 Y:\$07AE04,0,8 Y:\$07AE05,0,8 Y:\$07AE07,0,8	Y:\$07AF00,0,8 Y:\$07AF01,0,8 Y:\$07AF02,0,8 Y:\$07AF03,0,8 Y:\$07AF04,0,8 Y:\$07AF05,0,8 Y:\$07AF07,0,8	I/O bits 0-7 I/O bits 8-15 I/O bits 16-23 I/O bits 24-31 I/O bits 32-39 I/O bits 40-47 Control Word
SW1-3 OFF SW1-4 OFF	Y:\$07BC00,0,8 Y:\$07BC01,0,8 Y:\$07BC02,0,8 Y:\$07BC03,0,8 Y:\$07BC04,0,8 Y:\$07BC05,0,8 Y:\$078C07,0,8	Y:\$07BD00,0,8 Y:\$07BD01,0,8 Y:\$07BD02,0,8 Y:\$07BD03,0,8 Y:\$07BD04,0,8 Y:\$07BD05,0,8 Y:\$078D07,0,8	Y:\$07BE00,0,8 Y:\$07BE01,0,8 Y:\$07BE02,0,8 Y:\$07BE03,0,8 Y:\$07BE04,0,8 Y:\$07BE05,0,8 Y:\$078E07,0,8	Y:\$07BF00,0,8 Y:\$07BF01,0,8 Y:\$07BF02,0,8 Y:\$07BF03,0,8 Y:\$07BF04,0,8 Y:\$07BF05,0,8 Y:\$078F07,0,8	I/O bits 0-7 I/O bits 8-15 I/O bits 16-23 I/O bits 24-31 I/O bits 32-39 I/O bits 40-47 Control Word

Note: SW1-5 and SW1-6 must be set to ON

### Control Register

The control register at address {Base + 7} permits the configuration of the IOGATE IC to a variety of applications. The control register consists of 8 write/read-back bits – Bits 0 - 7. The control register consists of two sections; Direction Control and Register Select.

The direction control allows setting input bytes to be read only. One of the advantages of the IOGATE IC is the ability to define the bits as inputs or outputs. This “control” mechanism

allows you to ensure the inputs will always be read properly. Our traditional I/O accessories always define the inputs and outputs by hardware.

The register select bits allow you to define the input or output bytes inversion control or the latching input features.

### **Direction Control Bits**

Bits 0 to 5 of the control register simply control the direction of the I/O for the matching numbered data register. That is, Bit  $n$  controls the direction of the I/O at  $\{\text{Base} + n\}$ . A value of 0 in the control bit (the default) permits a write operation to the data register, enabling the output function for each line in the register. Enabling the output function does not prevent the use of any or all of the lines as inputs, as long as the outputs are off (non-conducting). A value of 1 in the control bit does not permit a write operation to the data register, disabling the output, reserving the register for inputs.

**Example:** A value of 1 in Bit 3 disables the write function into the data register at address  $\{\text{Base} + 3\}$ , ensuring that lines IO24 - IO31 can always be used as inputs.

### **Register Select Control Bits**

Bits 6 and 7 of the control register together select which of 4 possible registers can be accessed at each of the addresses  $\{\text{Base} + 0\}$  through  $\{\text{Base} + 5\}$ . They also select which of 2 possible registers can be selected at  $\{\text{Base} + 6\}$ .

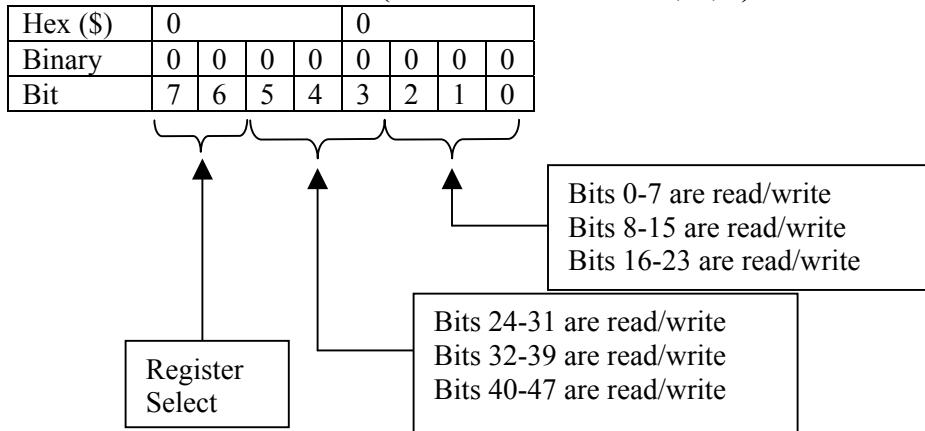
The following table explains how these bits select registers:

<b>Bit 7</b>	<b>Bit 6</b>	<b>Combined Value</b>	<b><math>\{\text{Base} + 0\}</math> to <math>\{\text{Base} + 5\}</math> Register Selected</b>	<b><math>\{\text{Base} + 6\}</math> Register Selected</b>
0	0	0	Data Register	Data Register
0	1	1	Setup Register 1	Setup Register
1	0	2	Setup Register 2	n. a.
1	1	3	Setup Register 3	n. a.

In a typical application, non-zero combined values of Bits 6 and 7 are used only for initial configuration of the IC. These values are used to access the setup registers at the other addresses. After the configuration is finished, zeros are written to both Bits 6 and 7, so the data registers at the other registers can be accessed.

### **Control Word Setup Example**

You need to set up the control words for the IO card at power up. To accomplish this task, a simple PLC could be written to set up the control word properly. For this example, we will be setting up one ACC-68E (IC0 - 24in/24out), one ACC66E (IC1 - 48 inputs), and one ACC-67E (IC2 - 48 outputs).

**Control Word for ACC-68E (M2007->Y:\$078C07,0,8)**

```

M2000->Y:$078C00,0,8          ;I/O bits 0-7 (port A IC0)
M2001->Y:$078C01,0,8          ;I/O bits 8-15 (port A IC0)
M2002->Y:$078C02,0,8          ;I/O bits 16-23 (port A IC0)
M2003->Y:$078C03,0,8          ;I/O bits 0-7 (port B IC0)
M2004->Y:$078C04,0,8          ;I/O bits 8-15 (port B IC0)
M2005->Y:$078C05,0,8          ;I/O bits 16-23 (port B IC0)
M2006->Y:$078C06,0,8          ;register selected
M2007->Y:$078C07,0,8          ;control register

M2008->Y:$078D00,0,8          ;I/O bits 0-7 (port A IC1)
M2009->Y:$078D01,0,8          ;I/O bits 8-15 (port A IC1)
M2010->Y:$078D02,0,8          ;I/O bits 16-23 (port A IC1)
M2011->Y:$078D03,0,8          ;I/O bits 0-7 (port B IC1)
M2012->Y:$078D04,0,8          ;I/O bits 8-15 (port B IC1)
M2013->Y:$078D05,0,8          ;I/O bits 16-23 (port B IC1)
M2014->Y:$078D06,0,8          ;register selected
M2015->Y:$078D07,0,8          ;control register

M2016->Y:$078E00,0,8          ;I/O bits 0-7 (port A IC2)
M2017->Y:$078E01,0,8          ;I/O bits 8-15 (port A IC2)
M2018->Y:$078E02,0,8          ;I/O bits 16-23 (port A IC2)
M2019->Y:$078E03,0,8          ;I/O bits 0-7 (port B IC2)
M2020->Y:$078E04,0,8          ;I/O bits 8-15 (port B IC2)
M2021->Y:$078E05,0,8          ;I/O bits 16-23 (port B IC2)
M2022->Y:$078E06,0,8          ;register selected
M2023->Y:$078E07,0,8          ;control register

M2007->Y:$078C07,0,8          ;control word for $78C00,0,8 - $78C05,0,8
M2015->Y:$078D07,0,8          ;control word for $78D00,0,8 - $78C05,0,8
M2023->Y:$078E07,0,8          ;control word for $78E00,0,8 - $78C05,0,8

;***** PLC to initialize read/write I/O bits *****
OPEN PLC 1 CLEAR
M2007=$07                      ;define bits 0-23 as inputs and bits 24-47 as outputs (ACC-68E)
M2015=$3F                        ;define bits 0-23 and 24-47 as inputs (ACC-66E)
M2023=$00                        ;define bits 0-23 and 24-47 as outputs (ACC-67E)
DIS PLC1
CLOSE

```

## **Accessory 68E I/O M-Variables for UMAC Turbo**

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The following is a list of suggested M-variables for the default jumper settings is provided. You may assign any M-variables to these addresses. You may make these M-variable definitions and use them as general purpose I/O for their PLC's or motion programs.

M7000->Y:\$078C00,0,1	Input 0	M7024->Y:\$078C03,0,1	Input 24
M7001->Y:\$078C00,1,1	Input 1	M7025->Y:\$078C03,1,1	Input 25
M7002->Y:\$078C00,2,1	Input 2	M7026->Y:\$078C03,2,1	Input 26
M7003->Y:\$078C00,3,1	Input 3	M7027->Y:\$078C03,3,1	Input 27
M7004->Y:\$078C00,4,1	Input 4	M7028->Y:\$078C03,4,1	Input 28
M7005->Y:\$078C00,5,1	Input 5	M7029->Y:\$078C03,5,1	Input 29
M7006->Y:\$078C00,6,1	Input 6	M7030->Y:\$078C03,6,1	Input 30
M7007->Y:\$078C00,7,1	Input 7	M7031->Y:\$078C03,7,1	Input 31
M7008->Y:\$078C01,0,1	Input 8	M7032->Y:\$078C04,0,1	Input 32
M7009->Y:\$078C01,1,1	Input 9	M7033->Y:\$078C04,1,1	Input 33
M7010->Y:\$078C01,2,1	Input 10	M7034->Y:\$078C04,2,1	Input 34
M7011->Y:\$078C01,3,1	Input 11	M7035->Y:\$078C04,3,1	Input 35
M7012->Y:\$078C01,4,1	Input 12	M7036->Y:\$078C04,4,1	Input 36
M7013->Y:\$078C01,5,1	Input 13	M7037->Y:\$078C04,5,1	Input 37
M7014->Y:\$078C01,6,1	Input 14	M7038->Y:\$078C04,6,1	Input 38
M7015->Y:\$078C01,7,1	Input 15	M7039->Y:\$078C04,7,1	Input 39
M7016->Y:\$078C02,0,1	Input 16	M7040->Y:\$078C05,0,1	Input 40
M7017->Y:\$078C02,1,1	Input 17	M7041->Y:\$078C05,1,1	Input 41
M7018->Y:\$078C02,2,1	Input 18	M7042->Y:\$078C05,2,1	Input 42
M7019->Y:\$078C02,3,1	Input 19	M7043->Y:\$078C05,3,1	Input 43
M7020->Y:\$078C02,4,1	Input 20	M7044->Y:\$078C05,4,1	Input 44
M7021->Y:\$078C02,5,1	Input 21	M7045->Y:\$078C05,5,1	Input 45
M7022->Y:\$078C02,6,1	Input 22	M7046->Y:\$078C05,6,1	Input 46
M7023->Y:\$078C02,7,1	Input 23	M7047->Y:\$078C05,7,1	Input 47

```
;***** Sample E-Stop PLC *****
; This PLC will abort all motion programs and kill the bus voltage to
; the motors when E-stop is depressed. When E-Stop button is pulled
; out
; the motors will servo to actual position (<ctrl> A command) after
; allowing 5 seconds for proper bus voltage.

;      P7000 used as a Latch variable
;      M7000 used Emergency Stop Input (from ACC-9E)
;      M8000 used as Main Contact for main AC for Bus Voltage (ACC-10E)
;      I5111 used as count down timer

OPEN PLC 5 CLEAR
IF (M7000=1 and P7000=0)      ;emergency stop condition
  CMD^A                      ;global motion program abort
  I5111=500*8388608/I10      ;500 msec delay for deceleration
  WHILE (I5111>0) ENDWHILE
  CMD^K                      ;kill all axes
  M8000=0                      ;turn off BUS voltage
  P7000=1                      ;latch input

Endif
IF (M7000=0 and P7000=1)
  M8000=1                      ;enable BUS volatge
  I5111=5000*8388608/I10      ;5000 msec delay for bus voltage
  WHILE (I5111>0) ENDWHILE
```

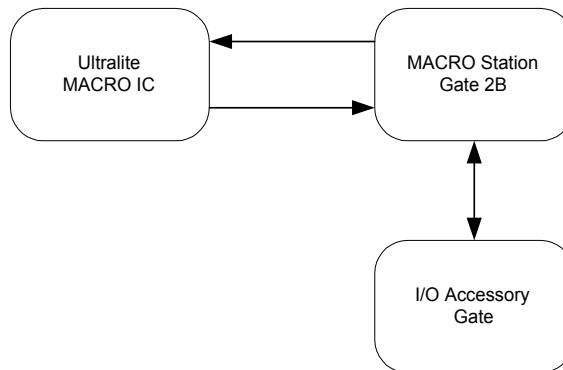
```
CMD^A          ;close loop for all servos
P7000=0        ;latch input
Endif
```

## MACRO-STATION I/O TRANSFER

A fundamental understanding of the MACRO Station I/O transfer is needed to set up the MACRO I/O family of accessories.

The MACRO station typically will have up to eight axis nodes (0, 1, 4, 5, 8, 9, 12, and 13) and up to six I/O transfer nodes (2, 3, 6, 7, 10, and 11). There are two types of I/O transfers allowed to send the information to the Ultralite from the MACRO-Station: 48-bit transfer and 24-bit transfer. The PMAC2 Ultralite and the MACRO-Station enable the user to transfer 72 bits per I/O node. For a multi Master system, 432 bits (6×72) of data may be transferred for each Master (Ultralite) in the ring. If only one Master is used in the ring, node 14 could be used for I/O transfer, which would give us 504 bits (7×72) of I/O transfer data.

For all MACRO-Station I/O accessories, the information is transferred to or from the accessory I/O Gate to the MACRO-Station CPU Gate 2B. Information from the MACRO-Station Gate 2B is then read or written directly to the MACRO IC on the Ultralite. Once the information is at the Ultralite, it can be used in the users application motion programs or PLC programs.



Each I/O board has jumper and software settings to select the I/O transfer memory locations at both the I/O transfer Gate and the MACRO transfer addresses. These jumpers and software settings are discussed in this manual.

### MACRO Station I/O Node Transfer Addresses

Node(s)	Node 24-bit: Transfer Addresses	Node 16-bit (upper 16 bits): Transfer Addresses
2	X:\$C0A0	X:\$C0A1, X:\$C0A2, X:\$C0A3
3	X:\$C0A4	X:\$C0A5, X:\$C0A6, X:\$C0A7
6	X:\$C0A8	X:\$C0A9, X:\$C0AA, X:\$C0AB
7	X:\$C0AC	X:\$C0AD, X:\$C0AD, X:\$C0AE
10	X:\$C0B0	X:\$C0B1, X:\$C0B2, X:\$C0B3
11	X:\$C0B4	X:\$C0B5, X:\$C0B6, X:\$C0B7

### PMAC2 Ultralite I/O Node Addresses

Node	Node 24-bit: Transfer Addresses	Node 16-bit (upper 16 bits): Transfer Addresses
2	X:\$C0A0	X:\$C0A1, X:\$C0A2, X:\$C0A3
3	X:\$C0A4	X:\$C0A5, X:\$C0A6, X:\$C0A7
6	X:\$C0A8	X:\$C0A9, X:\$C0AA, X:\$C0AB
7	X:\$C0AC	X:\$C0AD, X:\$C0AD, X:\$C0AE

10	X:\$C0B0	X:\$C0B1, X:\$C0B2, X:\$C0B3
11	X:\$C0B4	X:\$C0B5, X:\$C0B6, X:\$C0B7

### PMAC2 TURBO Ultralite I/O Node Addresses

MACR O IC Node	User Node	Node 24-bit: Transfer Addresses	Node 16-bit (upper 16 bits): Transfer Addresses
(IC0 ) 2	2	X:\$078420	X:\$078421, X:\$078422, X:\$078423
(IC0 ) 3	3	X:\$078424	X:\$078425, X:\$078426, X:\$078427
(IC0 ) 6	6	X:\$078428	X:\$078429, X:\$07842A, X:\$07842B
(IC0 ) 7	7	X:\$07842C	X:\$07842D, X:\$07842E, X:\$07842F
(IC0 ) 10	10	X:\$078430	X:\$078431, X:\$078432, X:\$078433
(IC0 ) 11	11	X:\$078434	X:\$078435, X:\$078436, X:\$078437
(IC1 ) 2	18	X:\$079420	X:\$079421, X:\$079422, X:\$079423
(IC1 ) 3	19	X:\$079424	X:\$079425, X:\$079426, X:\$079427
(IC1 ) 6	22	X:\$079428	X:\$079429, X:\$07942A, X:\$07942B
(IC1 ) 7	23	X:\$07942C	X:\$07942D, X:\$07942E, X:\$07942F
(IC1 ) 10	26	X:\$079430	X:\$079431, X:\$079432, X:\$079433
(IC1 ) 11	27	X:\$079434	X:\$079435, X:\$079436, X:\$079437
(IC2 ) 2	34	X:\$078420	X:\$07A421, X:\$07A422, X:\$07A423
(IC2 ) 3	35	X:\$07A424	X:\$07A425, X:\$07A426, X:\$07A427
(IC2 ) 6	38	X:\$07A428	X:\$07A429, X:\$07A42A, X:\$07A42B
(IC2 ) 7	39	X:\$07A42C	X:\$07A42D, X:\$07A42E, X:\$07A42F
(IC2 ) 10	42	X:\$07A430	X:\$07A431, X:\$07A432, X:\$07A433
(IC2 ) 11	43	X:\$07A434	X:\$07A435, X:\$07A436, X:\$07A437
(IC3 ) 2	50	X:\$07B420	X:\$07B421, X:\$07B422, X:\$07B423
(IC3 ) 3	51	X:\$07B424	X:\$07B425, X:\$07B426, X:\$07B427
(IC3 ) 6	54	X:\$07B428	X:\$07B429, X:\$07B42A, X:\$07B42B
(IC3 ) 7	55	X:\$07B42C	X:\$07B42D, X:\$07B42E, X:\$07B42F
(IC3 ) 10	58	X:\$07B430	X:\$07B431, X:\$07B432, X:\$07B433
(IC3 ) 11	59	X:\$07B434	X:\$07B435, X:\$07B436, X:\$07B437

**Example:** If the user wanted to read the inputs from the MACRO Station of the first 24-bit I/O node address of node 2 (X:\$C0A0), then he/she could point an M-variable to the Ultralite or TURBO Ultralite I/O node registers to monitor the inputs.

M980->X:\$C0A0,0,24

;Ultralite node2 address

M1980->X:\$078420,0,24

;TURBO Ultralite MACRO IC0 node 2 address

These M-variable definitions (M980 or M1980) could then be used to monitor the inputs for either the Ultralite or TURBO Ultralite, respectively.

## MACRO I/O SOFTWARE SETTINGS

The MACRO-Station I/O can be configured as either an input or an output. The hardware connected to the MACRO I/O boards determines whether or not the addresses defined are inputs or outputs. Each I/O node has 72-bits of data to be transferred automatically to the Ultralite. As stated previously, there are three methods of transfer: 3×16-bit, 1×24-bit, or 72-bit transfer.

There are several variables at the MACRO-Station and PMAC2 Ultralite that enable the I/O data transfer. Once these variables are set to the appropriate values, the user can then process the data like a normal PMAC or PMAC2. The variables to be modified at the MACRO-Station are MI19, MI69, MI70, or MI71.

To read multiple extended address UMAC IO cards efficiently, a new function was added to MACRO firmware 1.16 to read consecutive extended addresses. The previous method supported the low-middle-high byte addressing of the Type A IO cards (see Hardware Address Limitations section).

**MI19** controls the data transfer period on a Compact MACRO Station between the MACRO node interface registers and the I/O registers, as specified by station MI-variables MI20 through MI71. If MI19 is set to 0, this data transfer is disabled. If MI19 is greater than 0, its value sets the period in Phase clock cycles (the same as MACRO communications cycles) at which the transfer is done.

**MI975** permits the enabling of MACRO I/O nodes on the Compact MACRO Station. MI975 is a 16-bit value (bits 0 to 15) with bit  $n$  controlling the enabling of MACRO node  $n$ . If the bit is set to 0, the node is disabled; if the bit is set to 1, the node is enabled. The I/O nodes on the Compact MACRO Station are nodes 2, 3, 6, 7, 10, and 11, which can be enabled by MI975 bits of these numbers. Only bits 2, 3, 6, 7, 10, and 11 of MI975 should ever be set to 1.

MI975 is used at the power-on/reset of the Compact MACRO Station in combination with rotary switch SW1 and MI976 to determine which MACRO nodes are to be enabled. The net result can be read in Station variable MI996. To get a value of MI975 to take effect, the value must be saved (**MSSAVE{node}**) and the Station reset (**MS\$\$\${node}**).

Example: Set MI975 to enable nodes 2 and 3.

### MS0, I975 Set Number MACRO IO nodes to be enabled

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

**∴ MS0, I975=\$000C**

<b>MS0, MI975=\$4</b>	; Enable I/O Node 2 alone
<b>MS0, MI975=\$C</b>	; Enable I/O Nodes 2 & 3
<b>MS0, MI975=\$4C</b>	; Enable I/O Nodes 2, 3, & 6
<b>MS0, MI975=\$CC</b>	; Enable I/O Nodes 2, 3, 6, & 7
<b>MS0, MI975=\$4CC</b>	; Enable I/O Nodes 2, 3, 6, 7, & 10
<b>MS0, MI975=\$CCC</b>	; Enable I/O Nodes 2, 3, 6, 7, 10, & 11
<b>MS4, MI975=\$40</b>	; Enable I/O Node 6 alone
<b>MS4, MI975=\$C0</b>	; Enable I/O Nodes 6 & 7
<b>MS8, MI975=\$400</b>	; Enable I/O Node 10 alone
<b>MS8, MI975=\$C00</b>	; Enable I/O Nodes 10 & 11

**MI69 and MI70** specify the registers used in 16-bit I/O transfers between MACRO node interface registers and I/O registers on the MACRO Station I/O accessory board. They are used only if MI19 is greater than 0.

**Note**

The examples for the setup of MI69 and MI70 require MACRO firmware 1.16 and above.

MI69 and MI70 are 48-bit variables represented as 12 hexadecimal digits. The first 6 digits specify the number and address of 48-bit (3 x 16) real-time MACRO-node register sets to be used. The second 6 digits specify the number and address of 16-bit I/O sets on the MACRO Station I/O accessory board to be used. The individual digits are specified as follows:

Digit #	Possible Values	Description
1	0, 1, 2, 3	Number of MACRO I/O nodes to use (0 disables); this should also match the number of 48-bit I/O sets you intend to use (see Digit 7)
2	0	(Reserved for future use)
3-6	\$C0A1 (Node 2), \$C0A5 (Node 3), \$C0A9 (Node 6), \$C0AD (Node 7), \$C0B1 (Node 10), \$C0B5 (Node 11)	MACRO Station X Address of MACRO I/O node first of three 16-bit registers
7	0, 1, 2, 3	Number of 16-bit I/O sets to use (1x16, 2x16, 3x16; 0 disables)
8	1	Set to 1 for ACC-14E, ACC-68E, ACC-66E, ACC-67E consecutive address read (Base, +\$1000, +\$2000)
9-12	\$8800, \$8840 \$8880, \$88C0	MACRO Station Y Base Address of ACC-14E, ACC-68E, ACC-66E, ACC-67E,

When this function is active, the MACRO Station will copy values from the MACRO command (input) node registers to the I/O board addresses; it will copy values from the I/O board addresses to the MACRO feedback (output) node registers. Writing a '0' to a bit of the I/O board enables it as an input, letting the output pull high. Writing a '1' to a bit of the I/O board enables it as an output and pulls the output low.

**Example:**

(1) 48 bit I/O transfer using node 2 with IO card base address of \$8800

MS0, MI69=\$10C0A1318800

(2) 96 bit I/O transfer using nodes 2 and 3, with IO card base address of \$8800 and \$9800

MS0, MI69=\$20C0A1318800

(3) 288 bit I/O transfer using nodes 2, 3, 6, 7, 10, and 11 using 6 IO cards. Setup using 144-bit transfer with MI69 and 144-bit transfer with MI70. The first three IO cards are addressed at \$8800, \$9800, and \$A800. The second three IO cards are addressed at \$8840, \$9840, and \$A840.

MS0, MI69=\$30C0A1318800

MS0, MI70=\$30C0AD318840

**MI71** specifies the registers used in 24-bit I/O transfers between MACRO I/O node interface registers and I/O registers on the MACRO Station I/O accessory board. It is used only if MI19 is greater than 0.

**Note**

The examples for the setup of MI71 require MACRO firmware 1.16 and above.

MI71 is a 48-bit variable represented as 12 hexadecimal digits. The first 6 digits specify the number and address of 48-bit real-time MACRO-node register sets to be used. The second 6 digits specify the number and address of 48-bit I/O sets on the MACRO Station I/O accessory board to be used. The individual digits are specified as follows:

Digit #	Possible Values	Description
1	0, 1, 2, 3	Number of MACRO I/O nodes to use times 2 (0 disables); this should also match the number of 48-bit I/O sets you intend to use (see Digit 7)
2	0	(Reserved for future use)
3-6	\$C0A0 (Node 2), \$C0A4 (Node 3), \$C0A8 (Node 6), \$C0AC (Node 7), \$C0B0 (Node 10), \$C0B4 (Node 11)	MACRO Station X Address of MACRO I/O node first of three 16-bit registers
7	0, 1, 2	Number of 24-bit I/O sets to use (1x24, 2x24; 0 disables)
8	1	Set to 1 for ACC-14E, ACC-68E, ACC-66E, ACC-67E consecutive address read (Base, +\$1000, +\$2000)
9-12	\$8800, \$8840 \$8880, \$88C0	MACRO Station Y Base Address of ACC-14E, ACC-68E, ACC-66E, ACC-67E,

When this function is active, the MACRO Station will copy values from the MACRO command (input) node registers to the I/O board addresses; it will copy values from the I/O board addresses to the MACRO feedback (output) node registers. Writing a '0' to a bit of the I/O board enables it as an input, letting the output pull high. Writing a '1' to a bit of the I/O board enables it as an output and pulls the output low.

**Example:**

(1) 48 bit I/O transfer using nodes 2 and 3 with IO card base address of \$8800

MS0, MI71=\$10C0A01218800

(2) 96 bit I/O transfer using nodes 2, 3, 6, and 7 with IO card base address of \$8800 and \$9800

MS0, MI71=\$20C0A0218800

(3) 144-bit I/O transfer using nodes 2, 3, 6, 7, 10, and 11 using three IO cards at base address \$8800, \$9800 and \$A800.

MS0, MI71=\$30C0A0218800

## READING AND WRITING TO NODE ADDRESSES

Delta Tau recommends that you read and write to the node address as complete words. If the node address is 24-bits wide or 16-bits wide, read or write to the M-Variable assigned to that address:

### Example:

Ultralite	TURBO Ultralite
M970->X:\$C0A0,0,24	M970->X:\$78420,0,24
M980->X:\$C0A1,8,16	M980->X:\$78421,8,16
M981->X:\$C0A2,8,16	M981->X:\$78422,8,16
M982->X:\$C0A3,8,16	M982->X:\$78423,8,16
M1000->X:\$0770,0,24	M1000->X:\$0010F0,0,24 ;image word
M1001->X:\$0771,8,16	M1001->X:\$0010F0,8,16 ;image word
<b>For Outputs:</b>	
M970=\$F00011	;sets bits 0,4,20,21,22,& 23
M980=\$8101	;sets bits 0,8,& 23
M970=M1000	;sets M970 equal to M1000
M980=M1001	;sets M980 equal to M1001
<b>For Inputs:</b>	
M1000=M970	;sets M1000 equal to M970
M1001=M980	;sets M1001 equal to M980

If using the 48-bit read/write method, it would be ideal if the inputs and outputs were used in multiples of 16. Example: 48 inputs, 32 inputs, 16 outputs, 16 inputs 32 outputs, or 48 output (see **Example 2**).

If the 16-bit word is to be split (8 in and 8 out), then we would read the word at the beginning of the PLC and write the word at the end of the PLC. However, instead of writing the value of the inputs to the output word, you must write zeros to all input bits of this “in/out” word. This is because writing a value of 1 to a MACRO-I/O register makes that I/O bit an *output only* bit. The best method to ensure proper input reads is to write directly to the control word of the IO gate array to set the input words as read only (see Setting Up Control Word for MACRO IO section).

### Example Setup:

System Configuration: 8-axis PWM System w/ 96 bit I/O (48 inputs & 48 outputs)  
ACC-68E & ACC-68E

#### PMAC Ultralite Setup

I996=\$FB33F ;activates nodes 1,2,3,4,5,8,9,12, and 13 at Ultralite

#### TURBO PMAC Ultralite Setup

I6841=\$FB33F ;activates nodes 1,2,3,4,5,8,9,12, and 13 at Turbo Ultralite

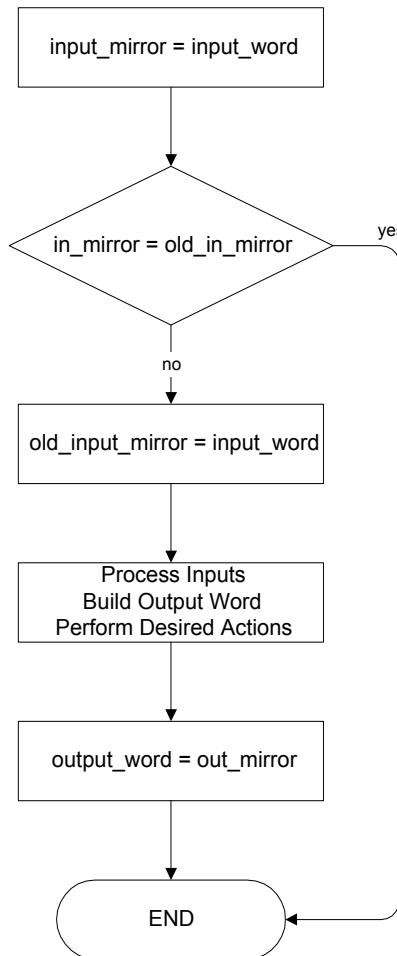
#### Macro Station Definitions:

MS0,MI69=\$20C0A1318800 ;sets up macro to transfer data for IO cards  
MS0,MI975=\$C ;enable node **2 and 3** for I/O  
MS0,MI19=4 ;sets interrupt period for data transfer  
MSSAVE0 ;save to macro station  
MS\$\$\$0 ;reset macro station to enable

### Active Nodes for Compact MACRO I/O Station (example)

Option	Node(s)	Gate Addresses	Node Transfer Addresses
48-Bit	2	\$8800	\$C0A1,\$C0A2,\$C0A3
96-Bit	2,3	\$8800 \$9800	\$C0A1,\$C0A2,\$C0A3 \$C0A5,\$C0A6,\$C0A7
144-Bit	2,3,6	\$8800 \$9800 \$A800	\$C0A1,\$C0A2,\$C0A3 \$C0A5,\$C0A6,\$C0A7 \$C0A9,\$C0AA,\$C0AB

The data in this application will transfer 48-bits of data per node as specified by MI69. These memory locations could be utilized by pointing an M-variable to the node locations. In your PLC program, these M-variables would be considered the actual input words and actual output words or a combination of the two (8 inputs/ 8 outputs for 16-bit read/write). To efficiently read and write to these memory locations, Delta Tau suggests using image input words to read the actual input words and then write to the actual output word if the inputs have changed states. The following block diagram shows the typical logic for PMAC's inputs and outputs.



For this application, we are using six 16-bit data transfers and will use the following M-Variable definitions in our application.

## PMAC2 Ultralite Example M-Variable Definitions

```

M980->X:$C0A1,8,16      ;IO word #1, 1st 16 bit word node2
M981->X:$C0A2,8,16      ;IO word #2, 2nd 16 bit word node 2
M982->X:$C0A3,8,16      ;IO word #3, 3rd 16 bit word node 2
M983->X:$C0A5,8,16      ;IO word #1, 1st 16 bit word node 3
M984->X:$C0A6,8,16      ;IO word #2, 2nd 16 bit word node 3
M985->X:$C0A7,8,16      ;IO word #3, 3rd 16 bit word node 3

M1000->X:$0770,8,16     ;Input mirror word #1
M1001->Y:$0770,8,16     ;Input mirror word #2
M1002->X:$0771,8,16     ;Input mirror word #3
M1003->Y:$0771,8,16     ;Output mirror word #1
M1004->X:$0772,8,16     ;Output mirror word #2
M1005->Y:$0772,8,16     ;Output mirror word #3
M1010->X:$0773,8,16     ;Old Image mirror word #1
M1011->Y:$0773,8,16     ;Old Image mirror word #2
M1012->X:$0774,8,16     ;Old Image mirror word #3

```

IO word #1	IO Word #2	IO Word #3
M800->X:\$770,8	M816->Y:\$770,8	M832->X:\$771,8
M801->X:\$770,9	M817->Y:\$770,9	M833->X:\$771,9
M802->X:\$770,10	M818->Y:\$770,10	M834->X:\$771,10
M803->X:\$770,11	M819->Y:\$770,11	M835->X:\$771,11
M804->X:\$770,12	M820->Y:\$770,12	M836->X:\$771,12
M805->X:\$770,13	M829->Y:\$770,13	M837->X:\$771,13
M806->X:\$770,14	M822->Y:\$770,14	M838->X:\$771,14
M807->X:\$770,15	M823->Y:\$770,15	M839->X:\$771,15
M808->X:\$770,16	M824->Y:\$770,16	M840->X:\$771,16
M809->X:\$770,17	M825->Y:\$770,17	M841->X:\$771,17
M810->X:\$770,18	M826->Y:\$770,18	M842->X:\$771,18
M811->X:\$770,19	M827->Y:\$770,19	M843->X:\$771,19
M812->X:\$770,20	M828->Y:\$770,20	M844->X:\$771,20
M813->X:\$770,21	M829->Y:\$770,21	M845->X:\$771,21
M814->X:\$770,22	M830->Y:\$770,22	M846->X:\$771,22
M815->X:\$770,23	M831->Y:\$770,23	M847->X:\$771,23

IO word #4	IO Word #5	IO Word #6
M900->Y:\$771,8	M916->X:\$772,8	M932->Y:\$772,8
M901->Y:\$771,9	M917->X:\$772,9	M933->Y:\$772,9
M902->Y:\$771,10	M918->X:\$772,10	M934->Y:\$772,10
M903->Y:\$771,11	M919->X:\$772,11	M935->Y:\$772,11
M904->Y:\$771,12	M920->X:\$772,12	M936->Y:\$772,12
M905->Y:\$771,13	M129->X:\$772,13	M937->Y:\$772,13
M906->Y:\$771,14	M922->X:\$772,14	M938->Y:\$772,14
M907->Y:\$771,15	M923->X:\$772,15	M939->Y:\$772,15
M908->Y:\$771,16	M924->X:\$772,16	M940->Y:\$772,16
M909->Y:\$771,17	M925->X:\$772,17	M941->Y:\$772,17
M910->Y:\$771,18	M926->X:\$772,18	M942->Y:\$772,18
M911->Y:\$771,19	M927->X:\$772,19	M943->Y:\$772,19
M912->Y:\$771,20	M928->X:\$772,20	M944->Y:\$772,20
M913->Y:\$771,21	M129->X:\$772,21	M945->Y:\$772,21
M914->Y:\$771,22	M930->X:\$772,22	M946->Y:\$772,22
M915->Y:\$771,23	M931->X:\$772,23	M947->Y:\$772,23

## PMAC2 TURBO Ultralite Example M-Variable Definitions

M980->X:\$78421,8,16	;IO word #1, 1 <sup>st</sup> 16 bit word node2
M981->X:\$78422,8,16	;IO word #2, 2 <sup>nd</sup> 16 bit word node 2
M982->X:\$78423,8,16	;IO word #3, 3 <sup>rd</sup> 16 bit word node 2
M983->X:\$78425,8,16	;IO word #1, 1 <sup>st</sup> 16 bit word node 3
M984->X:\$78426,8,16	;IO word #2, 2 <sup>nd</sup> 16 bit word node 3
M985->X:\$78427,8,16	;IO word #3, 3 <sup>rd</sup> 16 bit word node 3
M1000->X:\$0010F0,8,16	;Input mirror word #1
M1001->Y:\$0010F0,8,16	;Input mirror word #2
M1002->X:\$0010F1,8,16	;Input mirror word #3
M1003->Y:\$0010F1,8,16	;Output mirror word #1
M1004->X:\$0010F2,8,16	;Output mirror word #2
M1005->Y:\$0010F2,8,16	;Output mirror word #3
M1010->X:\$0010F3,8,16	;Old Image mirror word #1
M1011->Y:\$0010F3,8,16	;Old Image mirror word #2
M1012->X:\$0010F4,8,16	;Old Image mirror word #3

IO word #1	IO Word #2	IO Word #3
M800->X:\$0010F0,8	M816->Y:\$0010F0,8	M832->X:\$0010F1,8
M801->X:\$0010F0,9	M817->Y:\$0010F0,9	M833->X:\$0010F1,9
M802->X:\$0010F0,10	M818->Y:\$0010F0,10	M834->X:\$0010F1,10
M803->X:\$0010F0,11	M819->Y:\$0010F0,11	M835->X:\$0010F1,11
M804->X:\$0010F0,12	M820->Y:\$0010F0,12	M836->X:\$0010F1,12
M805->X:\$0010F0,13	M829->Y:\$0010F0,13	M837->X:\$0010F1,13
M806->X:\$0010F0,14	M822->Y:\$0010F0,14	M838->X:\$0010F1,14
M807->X:\$0010F0,15	M823->Y:\$0010F0,15	M839->X:\$0010F1,15
M808->X:\$0010F0,16	M824->Y:\$0010F0,16	M840->X:\$0010F1,16
M809->X:\$0010F0,17	M825->Y:\$0010F0,17	M841->X:\$0010F1,17
M810->X:\$0010F0,18	M826->Y:\$0010F0,18	M842->X:\$0010F1,18
M811->X:\$0010F0,19	M827->Y:\$0010F0,19	M843->X:\$0010F1,19
M812->X:\$0010F0,20	M828->Y:\$0010F0,20	M844->X:\$0010F1,20
M813->X:\$0010F0,21	M829->Y:\$0010F0,21	M845->X:\$0010F1,21
M814->X:\$0010F0,22	M830->Y:\$0010F0,22	M846->X:\$0010F1,22
M815->X:\$0010F0,23	M831->Y:\$0010F0,23	M847->X:\$0010F1,23

IO word #4	IO Word #5	IO Word #6
M900->Y:\$0010F1,8	M916->X:\$0010F2,8	M932->Y:\$0010F2,8
M901->Y:\$0010F1,9	M917->X:\$0010F2,9	M933->Y:\$0010F2,9
M902->Y:\$0010F1,10	M918->X:\$0010F2,10	M934->Y:\$0010F2,10
M903->Y:\$0010F1,11	M919->X:\$0010F2,11	M935->Y:\$0010F2,11
M904->Y:\$0010F1,12	M920->X:\$0010F2,12	M936->Y:\$0010F2,12
M905->Y:\$0010F1,13	M129->X:\$0010F2,13	M937->Y:\$0010F2,13
M906->Y:\$0010F1,14	M922->X:\$0010F2,14	M938->Y:\$0010F2,14
M907->Y:\$0010F1,15	M923->X:\$0010F2,15	M939->Y:\$0010F2,15
M908->Y:\$0010F1,16	M924->X:\$0010F2,16	M940->Y:\$0010F2,16
M909->Y:\$0010F1,17	M925->X:\$0010F2,17	M941->Y:\$0010F2,17
M910->Y:\$0010F1,18	M926->X:\$0010F2,18	M942->Y:\$0010F2,18
M911->Y:\$0010F1,19	M927->X:\$0010F2,19	M943->Y:\$0010F2,19
M912->Y:\$0010F1,20	M928->X:\$0010F2,20	M944->Y:\$0010F2,20
M913->Y:\$0010F1,21	M129->X:\$0010F2,21	M945->Y:\$0010F2,21
M914->Y:\$0010F1,22	M930->X:\$0010F2,22	M946->Y:\$0010F2,22
M915->Y:\$0010F1,23	M931->X:\$0010F2,23	M947->Y:\$0010F2,23

## Example 1: 48 inputs 48 outputs using 1x24-bit transfers

For this example, the inputs and outputs are not sharing the same Node Transfer Address (\$C0A0,\$C0A4,\$C0A8, \$C0AC). Each of the node transfer addresses can be defined as 24-bit addresses.

Ultralite (8 Axis)	Turbo Ultralite (8 Axis)	Description
I996=\$0FB3FF	I6841=\$0FB3FF	Enable nodes 0,1,2,3,4,5,6,7,8,9,12, & 13 at PMAC Ultralite
M970->X:\$C0A0,0,24	M970->X:\$78420,0,24	IO word #1, 24 bit word node2
M971->X:\$C0A4,0,24	M971->X:\$78424,0,24	IO word #2, 24 bit word node 3
M972->X:\$C0A8,0,24	M972->X:\$78428,0,24	IO word #3, 24 bit word node 6
M973->X:\$C0AC,0,24	M973->X:\$7842C,0,24	IO word #1, 24 bit word node 7
M1000->X:\$0770,0,24	M1000->X:\$0010F0,0,24	Input mirror word #1
M1001->Y:\$0770,0,24	M1001->Y:\$0010F0,0,24	Input mirror word #2
M1002->X:\$0771,0,24	M1002->X:\$0010F1,0,24	Output mirror word #1
M1003->Y:\$0771,0,24	M1003->Y:\$0010F1,0,24	Output mirror word #2
M1010->X:\$0772,0,24	M1010->X:\$0010F2,0,24	Old Input mirror word #2
M1011->Y:\$0772,0,24	M1011->Y:\$0010F2,0,24	Old Input mirror word #3

MS0,MI71=\$20C0A0218800 ;sets up macro to transfer data for ACC-68E and 66E  
 MS0,MI975=\$CC ;enable node **2, 3, 6, and 7** for I/O at MACRO Station  
 MS0,MI19=4 ;sets interrupt period for data transfer  
 MSSAVE0 ;save to macro station  
 MS\$\$\$0 ;reset macro station to enable

OPEN PLC1 CLEAR

M1000=M970 new input mirror equal to actual input word  
 M1001=M971 new input mirror equal to actual input word

IF (M1000 != M1010) OR (M1001 != M1011) if inputs change, process outputs

## Example 2: 48 inputs 48 outputs using $3 \times 16$ -bit transfers

For this example, the inputs and outputs are not sharing the same Node Transfer Address (\$C0A1,\$C0A2,\$C0A3, \$C0A5, \$C0A6, and \$C0A7). Each of the node transfer addresses can be defined as 16-bit addresses.

<b>Ultralite (8 Axis)</b>	<b>Turbo Ultralite (8 Axis)</b>	<b>Description</b>
I996=\$0FB33F	I6841=\$0FB33F	Enable nodes 0,1,2,3,4,5,8,9,12, & 13 at PMAC Ultralite
M980->X:\$C0A1,8,16	M980->X:\$78421,8,16	IO word #1, 1st 16 bit word node2
M981->X:\$C0A2,8,16	M981->X:\$78422,8,16	IO word #2, 2nd 16 bit word node 2
M982->X:\$C0A3,8,16	M982->X:\$78423,8,16	IO word #3, 3rd 16 bit word node 2
M983->X:\$C0A5,8,16	M983->X:\$78425,8,16	IO word #1, 1st 16 bit word node 3
M984->X:\$C0A6,8,16	M984->X:\$78426,8,16	IO word #2, 2nd 16 bit word node 3
M985->X:\$C0A7,8,16	M985->X:\$78427,8,16	IO word #3, 3rd 16 bit word node 3
M1000->X:\$0770,8,16	M1000->X:\$0010F0,8,16	Input mirror word #1
M1001->Y:\$0770,8,16	M1001->Y:\$0010F0,8,16	Input mirror word #2
M1002->X:\$0771,8,16	M1002->X:\$0010F1,8,16	Input mirror word #3
M1003->Y:\$0771,8,16	M1003->Y:\$0010F1,8,16	Output mirror word #1
M1004->X:\$0772,8,16	M1004->X:\$0010F2,8,16	Output mirror word #2
M1005->Y:\$0772,8,16	M1005->Y:\$0010F2,8,16	Output mirror word #3
M1010->X:\$0773,8,16	M1010->X:\$0010F3,8,16	Old Image mirror word #1
M1011->Y:\$0773,8,16	M1011->Y:\$0010F3,8,16	Old Image mirror word #2
M1012->X:\$0774,8,16	M1012->X:\$0010F4,8,16	Old Image mirror word #3

MS0.MI69=\$20C0A1318800 :sets up macro to transfer data for ACC-68E and 66E

MS0.MI975=\$C :enable node 2 and 3 for I/O

MS0.MI19=4 :sets interrupt period for data transfer

MSSAVE0 : save to macro station

MS\$##\$0 :reset macro station to enable

OPEN PI C1 CI FAR

M1000=M980  
M1001=M981

new input mirror equal to actual input word  
new input mirror equal to actual input word  
new input mirror equal to actual input word

IE (M1000  $\sqsubseteq$  M1010) OB (M1001  $\sqsubseteq$  M1011)

if inputs change process outputs

M1010 ≡ M1000

old input mirror equal to new input mirror

```
M1011 = M1001          old input mirror equal to new input mirror
:
:
:
M983 = M1003          Output word equals Output Mirror Word
M984 = M1004          Output word equals Output Mirror Word
M985 = M1005          Output word equals Output Mirror Word
ENDIF
CLOSE
```

**Set outputs based on inputs or program logic**

## **SETTING UP CONTROL WORD FOR MACRO IO**

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The Delta Tau IO gate array used on the UMAC IO accessories has the ability to allow any of the 48-bits be used as an input (read) or an output (write). To protect the inputs to be read only the user can define the individual bits as read only on a byte-by-byte basis. This accomplished by writing to the control word of the IO gate.

Each IO gate has eight 8-bit words:

IO word 0	- IO bits 0-7
IO word 1	- IO bits 8-15
IO word 2	- IO bits 16-23
IO word 3	- IO bits 24-31
IO word 4	- IO bits 32-39
IO word 5	- IO bits 40-47
IO word 6	- Data Word
IO word 7	<b>- Control Word</b>

IO words 0 through 5 contain the actual IO data. IO word 7 is the control word that allows us to turn any of the IO words into read only bits. The lower 6 bits of the Control Word are used to tell the IO gate whether or not the data in the six IO word bytes are read only or read/write registers. For example, if the user wanted to make IO word 0, IO word 1, and IO word 2 (bits 0-23) read only they would have to set the IO control word equal to 7 (binary 000111).

As of MACRO firmware release 1.16 there are no MI-variables to support direct access to the IO control words. An easy method can be used to write directly to the control word of the IO gate using MI198 and MI199 (place the register you want to read or write to into MI198 and the read or write to that value using MI199). This will usually be done in a one time read PLC at power up.

Base Address from SW1 Setting	Control Word Location	MI198 Setting
Y:\$8800	Y:\$8807,0,8	MI198=\$408807
Y:\$9800	Y:\$9807,0,8	MI198=\$409807
Y:\$A800	Y:\$A807,0,8	MI198=\$40A807
Y:\$B800 (\$FFE0*)	Y:\$B807,0,8	MI198=\$40B807
Y:\$8840	Y:\$8847,0,8	MI198=\$408847
Y:\$9840	Y:\$9847,0,8	MI198=\$409847
Y:\$A840	Y:\$A847,0,8	MI198=\$40A847
Y:\$B840 (\$FFE8*)	Y:\$B847,0,8	MI198=\$40B847
Y:\$8880	Y:\$8887,0,8	MI198=\$408887
Y:\$9880	Y:\$9887,0,8	MI198=\$409887
Y:\$A880	Y:\$A887,0,8	MI198=\$40A887
Y:\$B880 (\$FFF0*)	Y:\$B887,0,8	MI198=\$40B887
Y:\$88C0	Y:\$88C7,0,8	MI198=\$4088C7
Y:\$98C0	Y:\$98C7,0,8	MI198=\$4098C7
Y:\$A8C0	Y:\$A8C7,0,8	MI198=\$40A8C7
Y:\$B8C0	Y:\$B8C7,0,8	MI198=\$40B8C7

\* for legacy systems

Once we have the control word defined to MI198, we can write to the individual bytes associated with the IO gate and make them either read only or read/write (default).

Byte 0	Byte 1	Byte 2	Byte 3	Byte4	Byte 5
Y:\$8800,0,8	Y:\$8801,0,8	Y:\$8802,0,8	Y:\$8803,0,8	Y:\$8804,0,8	Y:\$8805,0,8
Y:\$9800,0,8	Y:\$9801,0,8	Y:\$9802,0,8	Y:\$9803,0,8	Y:\$9804,0,8	Y:\$9805,0,8

**Example: MACRO Station has ACC-68E (24in/24out) and ACC-66E(48 in) set to base addresses \$8800 and \$9800 respectively.**

```
#define Timer1 I5111      ;plc countdown timer for Turbo Ultralite
;#define Timer1 M70        ;plc countdown timer for Ultralite
;M70->X:$0700,0,24,s    ;countdown timer for non-turbo PMAC

Open PLC 10 Clear
Timer1=2000*8388608/I10      ;2 second delay to ensure MACRO
While (Timer1>0) Endwhile    ;Station is powered up properly

CMD"MS0,MI198=$408807"      ;set control word for ACC-68E
CMD"MS0,MI199=$07"          ;write $07 into Y:$8807 (control word)
Timer1=50*8388608/I10        ;50 msec delay
While (Timer1>0) Endwhile

CMD"MS0,MI198=$409807"      ;set control word for ACC-66E
CMD"MS0,MI199=$3F"          ;write $3F into Y:$9807 (control word)
Timer1=50*8388608/I10        ;50 msec delay
While (Timer1>0) Endwhile

Disable PLC10

Close
```

## LEGACY MACRO SYSTEMS

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The legacy systems are defined as MACRO CPU with the following part numbers:

- 602804-100
- 602804-101
- 602804-102
- 602804-103
- 602804-104

These systems do not have the extended addressing of the newer model MACRO CPU's (602804-105 through 602804-109). The addressing scheme for the legacy MACRO systems is listed below.

**The ACC-9E, ACC-10E, ACC-11E, and ACC-12E will have the following table**

### E1-E4: I/O Gate Transfer Jumpers

Jumper	UMAC MACRO
E1	\$8800 or \$FFE0
E2	\$8840 or \$FFE8
E3	\$8880 or \$FFF0
E4	\$88C0

The ACC-68E, ACC-66E, and ACC-67E are not direct replacements for ACC-9E, ACC-10E, and ACC-11E IO cards. The reason the self-protected IO is not a direct replacement is because of the addressing scheme. The older IO cards used the LOW, MIDDLE, and HIGH bytes of a base address and the MACRO I-variables would read consecutive IO cards in this manner. The self-protected IO cards are addressed from the LOW bytes only. Because of this, the MACRO I-variables (MI69, MI70, and MI71) were modified to read up to three consecutive base address cards in MACRO firmware version 1.16.

Chip Select	MACRO Address	DIP SWITCH SW1 POSITION					
		6	5	4	3	2	1
CS 10	\$FFE0	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
CS 12	\$FFE8	OPEN	OPEN	OPEN	OPEN	CLOSE	OPEN
CS 14	\$FFF0	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSE
CS 16	Cannot Use	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN

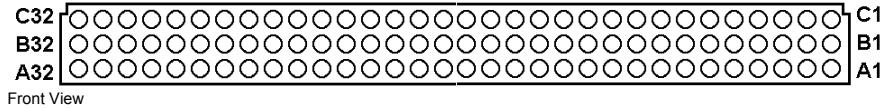
To use the new IO cards with the older firmware systems, the user can use each of the IO transfer variables (MI69, MI70, MI71) to transfer 48-bits each. The main problem is that the older systems did not have the new extended addressing and the user can only use **three** IO cards per MACRO station.

- For systems with only one IO card the user will not have to change anything
- If any of these New IO cards are used with the ACC-9E, ACC-10E, ACC-11E, or ACC-12E, then the user should address the New IO card as the first card (LOW byte) in addressing scheme.



## MACRO I/O ACCESSORY CONNECTORS

### P1 UBUS (96-PIN HEADER)



Pin #	Row A	Row B	Row C
1	+5Vdc	+5Vdc	+5Vdc
2	GND	GND	GND
3	BD01	DAT0	BD00
4	BD03	SEL0	BD02
5	BD05	DAT1	BD04
6	BD07	SEL1	BD06
7	BD09	DAT2	BD08
8	BD11	SEL2	BD10
9	BD13	DAT3	BD12
10	BD15	SEL3	BD14
11	BD17	DAT4	BD16
12	BD19	SEL4	BD18
13	BD21	DAT5	BD20
14	BD23	SEL5	BD22
15	BS1	DAT6	BS0
16	BA01	SEL6	BA00
17	BA03	DAT7	BA02
18	BX/Y	SEL7	BA04
19	CS3-	BA06	CS2-
20	BA05	BA07	CS4-
21	CS12-	BA08	CS10-
22	CS16-	BA09	CS14-
23	BA13	BA10	BA12
24	BRD-	BA11	BWR-
25	BS3	MEMCS0-	BS2
26	WAIT-	MEMCS1-	RESET
27	PHASE+	IREQ1-	SERVO+
28	PHASE-	IREQ2-	SERVO-
29	ANALOG	GND IREQ3-	ANALOG GND
30	-15Vdc	PWRGND	+15Vdc
31	GND	GND	GND
32	+5Vdc	+5Vdc	+5Vdc

For more details about the JEXP please see the UBUS Specification Document.

## I/O Terminals

TB1 Top (12-Pin Terminal Block)			Top View	
Pin #	Symbol	Function	Description	Notes
1	IN00	Input	Input #1	Sinking
2	IN01	Input	Input #2	Sinking
3	IN02	Input	Input #3	Sinking
4	IN03	Input	Input #4	Sinking
5	IN04	Input	Input #5	Sinking
6	IN05	Input	Input #6	Sinking
7	IN06	Input	Input #7	Sinking
8	IN07	Input	Input #8	Sinking
9	IN08	Input	Input #9	Sinking
10	IN09	Input	Input #10	Sinking
11	IN10	Input	Input #11	Sinking
12	IN11	Input	Input #12	Sinking

This terminal block provides the inputs 1-12 for the ACC-68E I/O Card.

TB2 Top (12-Pin Terminal Block)			Top View	
Pin #	Symbol	Function	Description	Notes
1	IN12	Input	Input #13	Sinking
2	IN13	Input	Input #14	Sinking
3	IN14	Input	Input #15	Sinking
4	IN15	Input	Input #16	Sinking
5	IN16	Input	Input #17	Sinking
6	IN17	Input	Input #18	Sinking
7	IN18	Input	Input #19	Sinking
8	IN19	Input	Input #20	Sinking
9	IN20	Input	Input #21	Sinking
10	IN21	Input	Input #22	Sinking
11	IN22	Input	Input #23	Sinking
12	IN23	Input	Input #24	Sinking

This terminal block provides the inputs 13-24 for the ACC-68E I/O Card.

TB3 Top (3-Pin Terminal Block)			Top View	
Pin #	Symbol	Function	Description	Notes
1	REF1	Reference	Reference Voltage for Inputs 1-8	24V for Sinking
2	REF2	Reference	Reference Voltage for Inputs 9-16	24V for Sinking
3	REF3	Reference	Reference Voltage for Inputs 17-24	24V for Sinking

This connector can be used to provide the input reference for the ACC-68E I/O Card for the 24 inputs.

TB1 Bottom (12-Pin Terminal Block)			Top View	
Pin #	Symbol	Function	Description	Notes
1	OUT00	Output	Output #1	Sinking
2	OUT01	Output	Output #2	Sinking
3	OUT02	Output	Output #3	Sinking
4	OUT03	Output	Output #4	Sinking
5	OUT04	Output	Output #5	Sinking
6	OUT05	Output	Output #6	Sinking
7	OUT06	Output	Output #7	Sinking
8	OUT07	Output	Output #8	Sinking
9	OUT08	Output	Output #9	Sinking
10	OUT09	Output	Output #10	Sinking
11	OUT10	Output	Output #11	Sinking
12	OUT11	Output	Output #12	Sinking

This terminal block provide the inputs 1-12 for the ACC-68E I/O Card

TB2 Bottom (12-Pin Terminal Block)			Top View	
Pin #	Symbol	Function	Description	Notes
1	OUT12	Output	Output #13	Sinking
2	OUT13	Output	Output #14	Sinking
3	OUT14	Output	Output #15	Sinking
4	OUT15	Output	Output #16	Sinking
5	OUT16	Output	Output #17	Sinking
6	OUT17	Output	Output #18	Sinking
7	OUT18	Output	Output #19	Sinking
8	OUT19	Output	Output #20	Sinking
9	OUT20	Output	Output #21	Sinking
10	OUT21	Output	Output #22	Sinking
11	OUT22	Output	Output #23	Sinking
12	OUT23	Output	Output #24	Sinking

This terminal block provides the inputs 13-24 for the ACC-68E I/O Card

TB3 Bottom (3-Pin Terminal Block)			Top View	
Pin #	Symbol	Function	Description	Notes
1	O+24V	Voltage	12-24V	
2	OGND	Reference	Reference voltage	
3	O+24V	Voltage	12-24V	

This terminal block can be used to provide the input reference for the ACC-68E for the 24 outputs



## DB15 CONNECTOR OPTION

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### DB15 Style Connector J1 Top – Inputs 1 through 12

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J1 Top Connector			Front View	
Pin #	Symbol	Function	Description	Notes
1	IN00	Input	Input #1	Sinking
2	IN02	Input	Input #3	Sinking
3	IN04	Input	Input #5	Sinking
4	IN06	Input	Input #7	Sinking
5	IN08	Input	Input #9	Sinking
6	IN10	Input	Input #11	Sinking
7	REF1	Reference	Reference Voltage for Inputs 1-8	24V for Sinking
8	REF2	Reference	Reference Voltage for Inputs 9-16	24V for Sinking
9	IN01	Input	Input #2	Sinking
10	IN03	Input	Input #4	Sinking
11	IN05	Input	Input #6	Sinking
12	IN07	Input	Input #8	Sinking
13	IN09	Input	Input #10	Sinking
14	IN11	Input	Input #12	Sinking
15	REF3	Reference	Reference Voltage for Inputs 17-24	24V for Sinking

## DB15 Style Connector J2 Top – Inputs 12 through 24

J2 Top Connector			Front View	
Pin #	Symbol	Function	Description	Notes
1	IN12	Input	Input #13	Sinking
2	IN14	Input	Input #15	Sinking
3	IN16	Input	Input #17	Sinking
4	IN18	Input	Input #19	Sinking
5	IN20	Input	Input #21	Sinking
6	IN22	Input	Input #23	Sinking
7	REF1	Reference	Reference Voltage for Inputs 1-8	24V for Sinking
8	REF2	Reference	Reference Voltage for Inputs 9-16	24V for Sinking
9	IN13	Input	Input #14	Sinking
10	IN15	Input	Input #16	Sinking
11	IN17	Input	Input #18	Sinking
12	IN19	Input	Input #20	Sinking
13	IN21	Input	Input #22	Sinking
14	IN23	Input	Input #24	Sinking
15	REF3	Reference	Reference Voltage for Inputs 17-24	24V for Sinking

## DB15 Style Connector J1 Bottom – Outputs 1 through 12

J1 Bottom Connector			Front View	
Pin #	Symbol	Function	Description	Notes
1	OUT00	Output	Output #1	Sinking
2	OUT02	Output	Output #3	Sinking
3	OUT04	Output	Output #5	Sinking
4	OUT06	Output	Output #7	Sinking
5	OUT08	Output	Output #9	Sinking
6	OUT10	Output	Output #11	Sinking
7	O+24V	Voltage	12-24V	
8	OGND	Reference	Reference voltage	
9	OUT01	Output	Output #2	Sinking
10	OUT03	Output	Output #4	Sinking
11	OUT05	Output	Output #6	Sinking
12	OUT07	Output	Output #8	Sinking
13	OUT09	Output	Output #10	Sinking
14	OUT11	Output	Output #12	Sinking
15	O+24V	Voltage	12-24V	

## DB15 Style Connector J2 Bottom – Outputs 12 through 24

J2 Bottom Connector			Front View	
Pin #	Symbol	Function	Description	Notes
1	OUT12	Output	Output #13	Sinking
2	OUT14	Output	Output #15	Sinking
3	OUT16	Output	Output #17	Sinking
4	OUT18	Output	Output #19	Sinking
5	OUT20	Output	Output #21	Sinking
6	OUT22	Output	Output #23	Sinking
7	O+24V	Voltage	12-24V	
8	OGND	Reference	Reference voltage	
9	OUT13	Output	Output #14	Sinking
10	OUT15	Output	Output #16	Sinking
11	OUT17	Output	Output #18	Sinking
12	OUT19	Output	Output #20	Sinking
13	OUT21	Output	Output #22	Sinking
14	OUT23	Output	Output #24	Sinking
15	O+24V	Voltage	12-24V	